CLAIMS

1. Apparatus for texture mapping in a computer graphics system, using a predetermined set of standardised textures, the apparatus having an input to receive data identifying one of the set of standardised textures, and means for processing the data to generate output texels of the identified texture; characterised in that each texture of the standardised set is a procedural texture, the input identifying data comprises one or a sequence of program commands the execution of which will result in the generation of a respective procedural texture, with the means for processing data comprising a processor operable to implement all such input program commands or sequences of input programme commands as required to generate the procedural textures of the standardised set.

2. Apparatus as claimed in Claim 1, having at least one further input for one or more predetermined classes of numerical parameter, with the processor being arranged to generate procedural textures with reference to the or each numerical parameter value received.

3. Apparatus as claimed in Claim 1, having at least one further input for a scale factor, with the processor being arranged to generate a procedural texture at a resolution determined by a received scale factor.

4. Apparatus as claimed in Claim 1, wherein the processor is operable to implement only such input program commands or sequences of input ~~programme~~ program commands as required to generate those procedural textures of the ~~standardised~~ standardised set.

5. Apparatus as claimed in Claim 1, further comprising a cache memory coupled with the processor, with the processor being configured to generate said procedural textures as texture maps within said cache.

6. Apparatus as claimed in Claim 5, further comprising an input to receive a scale factor, and an interpolator to generate output texels from texture map entries in the cache at a resolution determined by the received scale factor.

7. A semiconductor chip comprising a texture mapping apparatus as claimed in Claim 4 on a single substrate.

8. A semiconductor chip comprising a texture mapping apparatus as claimed in Claim 6, with the processor, cache and interpolator on a common substrate.

9. A computer graphics system including an apparatus as claimed in Claim 1, together with a source of three-dimensional polygon data, a geometry processor coupled to receive said polygon data and arranged to generate a two-dimensional representation of said polygons, a source of program commands coupled to the input of the texture mapping apparatus and specifying textures to be applied to respective ones of said polygons, and rendering means coupled to receive the outputs of the geometry processor and texture mapping apparatus and arranged to generate an output image of said polygons with texture applied.

10. A computer graphics system as claimed in Claim 9, wherein the sources of polygon data and program commands comprise an interface to a data network to which are coupled remote sources of such polygon data and program commands, the interface being coupled with a memory holding a store of network addresses for such remote sources and being operable to format and transmit messages to such addresses calling for the polygon data and program commands.

11. A computer graphics system as claimed in Claim 10, wherein said

program commands are transmitted over the network in virtual machine code and the system further comprises means for conversion of the ~~same~~ program commands to a local machine code supported by the processor.